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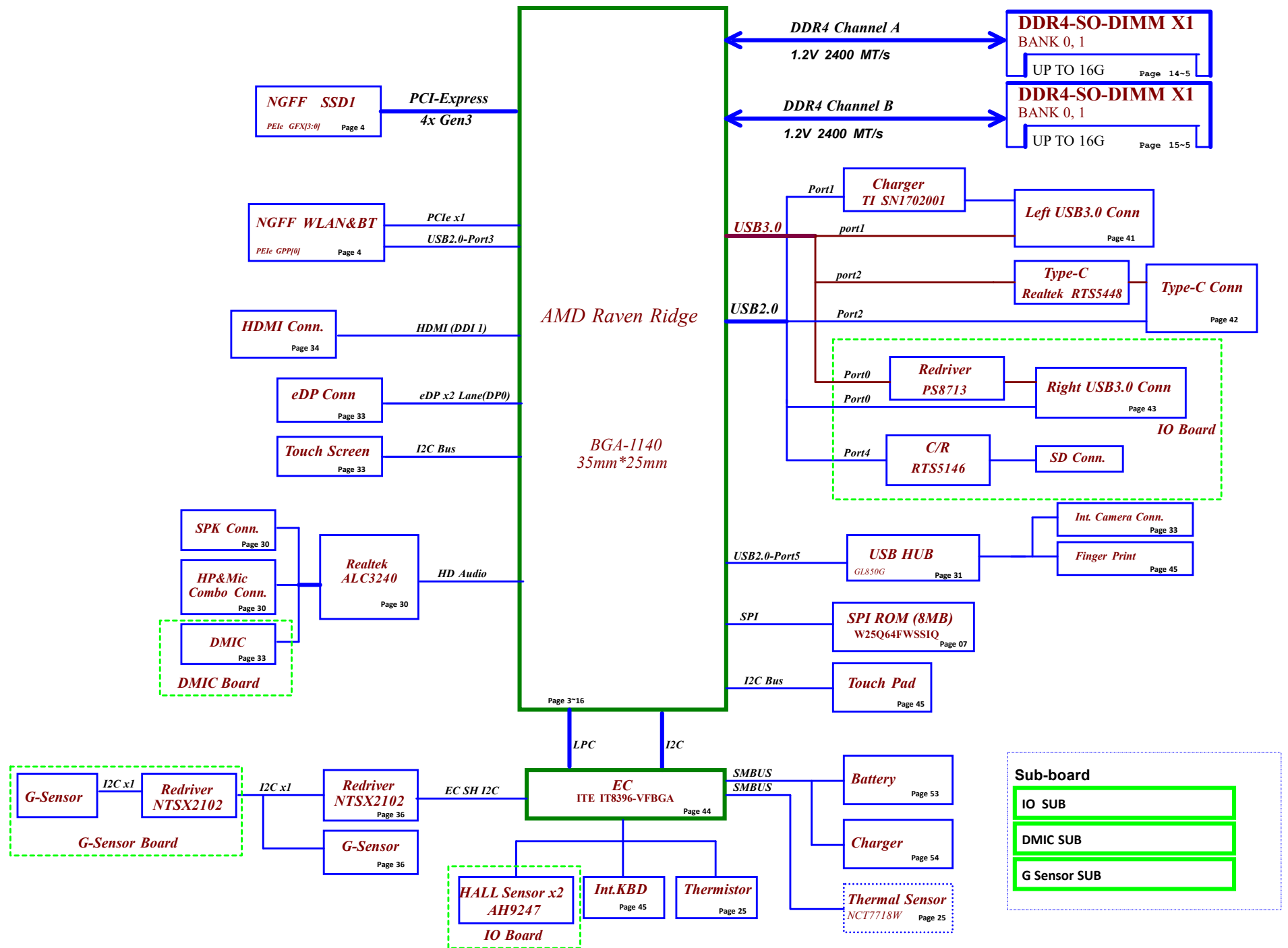
NM_B781 MB Schematics Document

AMD Raven Ridge with DDR4

2017-11

REV:1.0

Security Classification	LC Future Center Secret Data		Title			
Issued Date	2015/08/20	Deciphered Date	2016/08/20	Cover Page		
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power plane State	V20B+ +3VL +5VLP	+5VALW +3VALW (+3VALW APU) +1.8VALW +0.9VALW	+1.2V	+5VS +3VS +1.8VS +0.9VS +0.6VS +2.5VS +VDDC_VDD +VDDCR_SOC
S0	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

Port List


BOM Structure Table

SMBUS Control Table

	SOURCE	IT8396	TP	TS	SODIMM	WLAN
I2C0_CK I2C0_DA	APU VDD_18_S5	V	X	X	X	X
I2C1_CK I2C1_DA	APU VDD_18_S5	X	V	X	X	X
I2C2_CK I2C2_DA	APU VDD_33	X	X	X	V	V
I2C3_CK I2C3_DA	APU VDD_33_S5	X	X	V	X	X

EC SM Bus3 address

APU SM Bus address

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M.2 SSD1

26 PCIE_CRX_DTX_P0
26 PCIE_CRX_DTX_N0
26 PCIE_CRX_DTX_P1
26 PCIE_CRX_DTX_N1
26 PCIE_CRX_DTX_P2
26 PCIE_CRX_DTX_N2
26 PCIE_CRX_DTX_P3
26 PCIE_CRX_DTX_N3

PCIE_CRX_DTX_P0
PCIE_CRX_DTX_N0
PCIE_CRX_DTX_P1
PCIE_CRX_DTX_N1
PCIE_CRX_DTX_P2
PCIE_CRX_DTX_N2
PCIE_CRX_DTX_P3
PCIE_CRX_DTX_N3

P8
P9
N6
N7
M8
M9
L6
L7

P_GFX_RXP0
P_GFX_RXN0
P_GFX_RXP1
P_GFX_RXN1
P_GFX_RXP2
P_GFX_RXN2
P_GFX_RXP3
P_GFX_RXN3

P_GFX_TXP0
P_GFX_TXN0
P_GFX_TXP1
P_GFX_TXN1
P_GFX_TXP2
P_GFX_TXN2
P_GFX_TXP3
P_GFX_TXN3

N1
N3
M2
M4
L2
L4
L1
L3

PCIE_CTX_DRX_P0
PCIE_CTX_DRX_N0
PCIE_CTX_DRX_P1
PCIE_CTX_DRX_N1
PCIE_CTX_DRX_P2
PCIE_CTX_DRX_N2
PCIE_CTX_DRX_P3
PCIE_CTX_DRX_N3

PCIE_CTX_DRX_P0
PCIE_CTX_DRX_N0
PCIE_CTX_DRX_P1
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PCIE_CTX_DRX_P2
PCIE_CTX_DRX_N2
PCIE_CTX_DRX_P3
PCIE_CTX_DRX_N3

M.2 SSD1

WLAN

29 PCIE_PRX_DTX_P0
29 PCIE_PRX_DTX_N0

PCIE_PRX_DTX_P0
PCIE_PRX_DTX_N0

N10
N9

P_GPP_RXP0
P_GPP_RXN0

P_GPP_TXP0
P_GPP_TXN0

N2
P3

PCIE_PTX_DRX_P0
PCIE_PTX_DRX_N0

PCIE_PTX_C_DRX_P0
PCIE_PTX_C_DRX_N0

PCIE_PTX_C_DRX_P0
PCIE_PTX_C_DRX_N0

WLAN

SATA

24 SATA_PRX_DTX_P0
24 SATA_PRX_DTX_N0

SATA_PRX_DTX_P0
SATA_PRX_DTX_N0

R6
R7

P_GPP_RXP6/SATA_RXP0
P_GPP_RXN6/SATA_RXN0

P_GPP_TXP6/SATA_TXP0
P_GPP_TXN6/SATA_TXN0

V1
V3

SATA_PTX_DRX_P0
SATA_PTX_DRX_N0

SATA_PTX_DRX_P0
SATA_PTX_DRX_N0

24
24

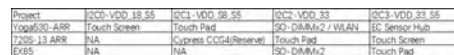


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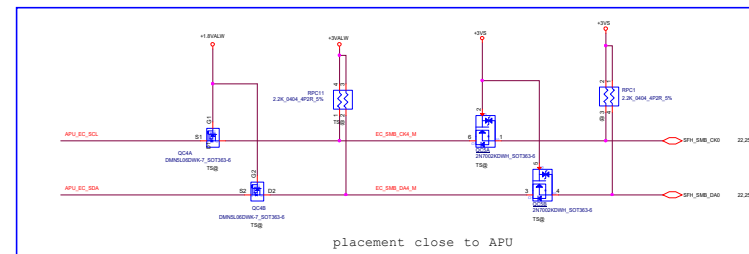
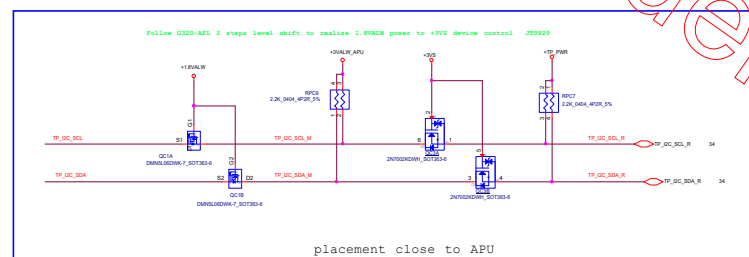
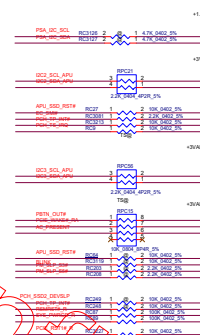
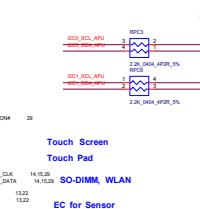
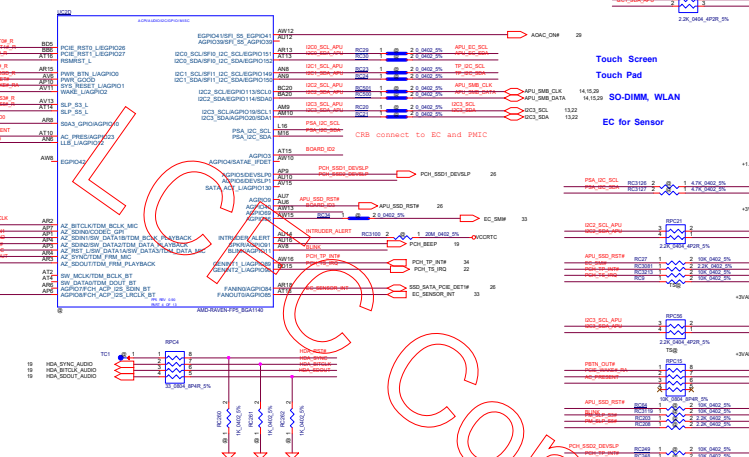
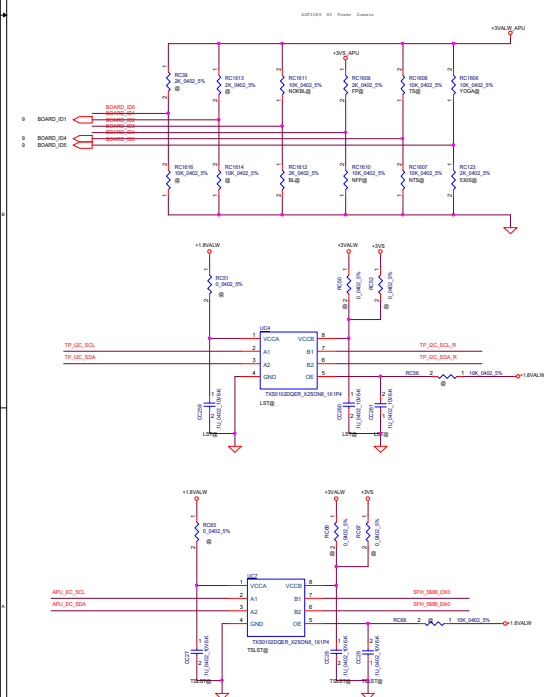
Title		Rev	
FP5 (PCIE SATA I/F)		1.0	
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Custom	YOGA530-ARR		
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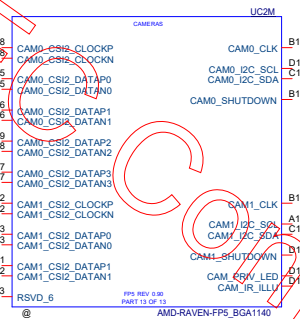






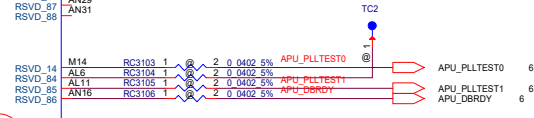
Board ID	Description	Staff #
Board_ID0	0 Reserved	NC1616
	1 Reserved	NC39
Board_ID1	0 SATA HDD	NC1614
	1 PATA HDD	NC1613
Board_ID2	0 EBL	NC1612
	1 ROM-EML	NC1611
Board_ID3	0 Rom-FF	NC1610
	1 FF	NC1609
Board_ID4	0 Rom-TS	NC1607
	1 TS	NC1606
Board_ID5	0 S3D5	NC1213
	1 V3D4	NC1606

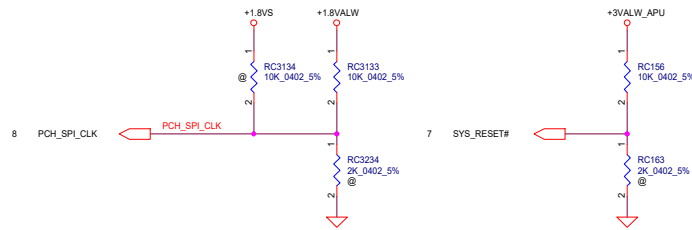




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				Rev	1.0

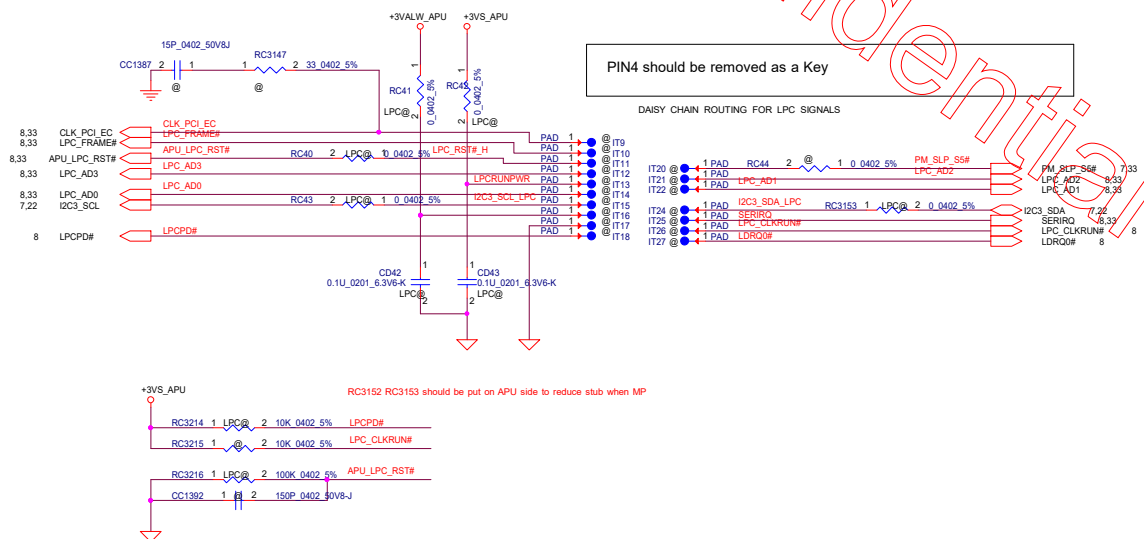






STRAP PINS	SYS_RESET#
PCH_SPI_CLK	1:USE 48MHZ CRYSTAL CLOCK AND GENERATE BOTH INTERNAL AND EXTERNAL CLOCKS (DEFAULT) 0:USE 100MHZ PCIE CLOCK AS REFERENCE CLOCK AND GENERATE INTERNAL CLOCKS ONLY
SYS_RESET#	1:NORMAL RESET MODE (DEFAULT) 0:SHORT RESET MODE

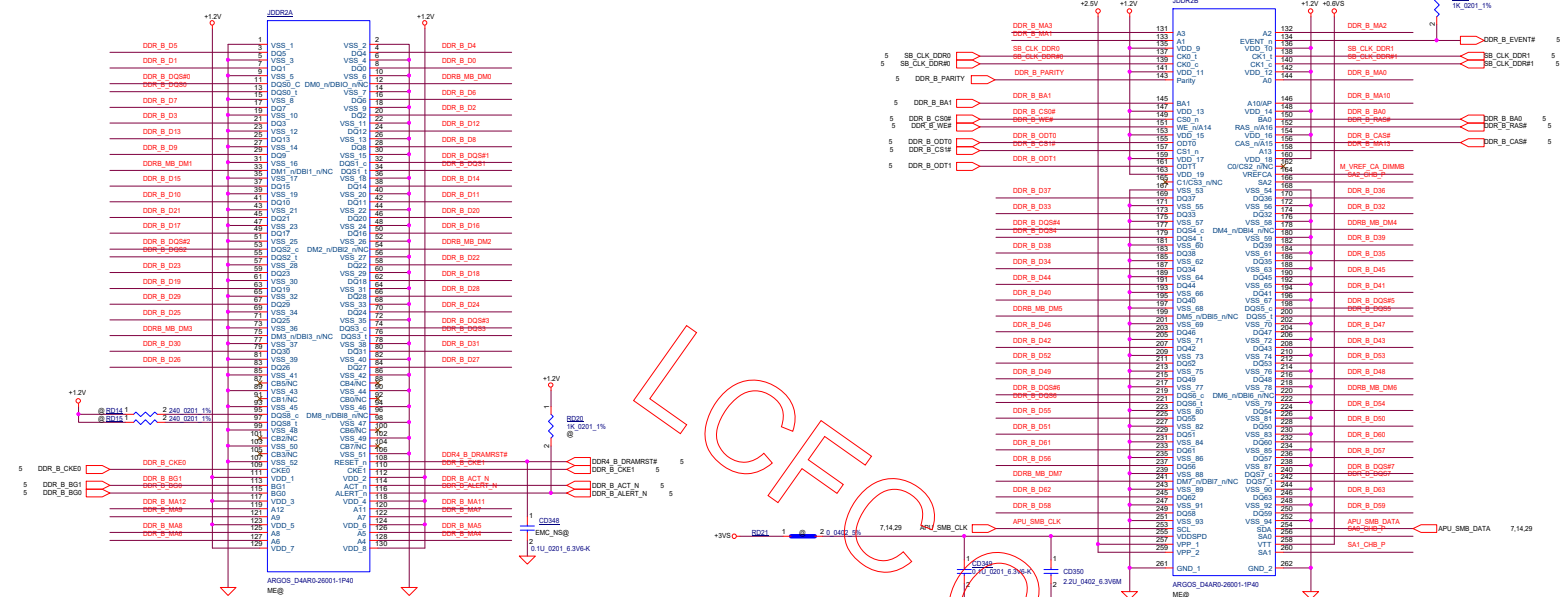
LPC ROM EMULATOR HEADER





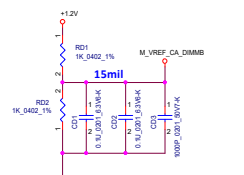
Swap Table

Pin Name	Net Name
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DQ1	DDRA_DQ5
DQ2	DDRA_DQ3
DQ3	DDRA_DQ3
DQ4	DDRA_DQ4
DQ5	DDRA_DQ5
DQ6	DDRA_DQ1
DQ7	DDRA_DQ8#0
DQ8#0	DDRA_DQ8#0
DQ8#0	DDRA_DQ8#0
DQ8	DDRA_DQ12
DQ9	DDRA_DQ13
DQ10	DDRA_DQ14
DQ11	DDRA_DQ15
DQ12	DDRA_DQ9
DQ13	DDRA_DQ8
DQ14	DDRA_DQ15
DQ15	DDRA_DQ11
DQ8#1	DDRA_DQ8#1
DQ8#1	DDRA_DQ8#1
DQ16	DDRA_DQ20
DQ17	DDRA_DQ21
DQ18	DDRA_DQ22
DQ19	DDRA_DQ19
DQ20	DDRA_DQ16
DQ21	DDRA_DQ17
DQ22	DDRA_DQ23
DQ23	DDRA_DQ18
DQ8#2	DDRA_DQ8#2
DQ8#2	DDRA_DQ8#2
DQ24	DDRA_DQ25
DQ25	DDRA_DQ26
DQ26	DDRA_DQ27
DQ27	DDRA_DQ28
DQ28	DDRA_DQ29
DQ29	DDRA_DQ30
DQ30	DDRA_DQ31
DQ31	DDRA_DQ32
DQ8#3	DDRA_DQ8#3
DQ8#3	DDRA_DQ8#3
DQ32	DDRA_DQ37
DQ33	DDRA_DQ38
DQ34	DDRA_DQ39
DQ35	DDRA_DQ40
DQ36	DDRA_DQ41
DQ37	DDRA_DQ42
DQ38	DDRA_DQ43
DQ39	DDRA_DQ44
DQ8#4	DDRA_DQ8#4
DQ8#4	DDRA_DQ8#4
DQ40	DDRA_DQ45
DQ41	DDRA_DQ46
DQ42	DDRA_DQ47
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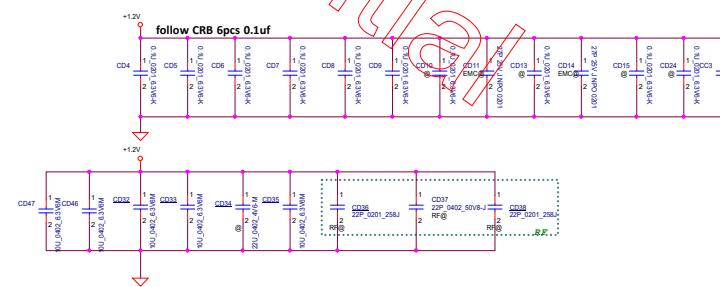
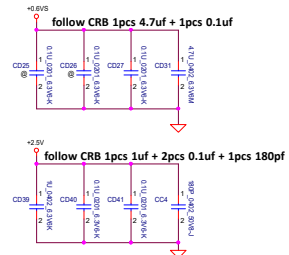


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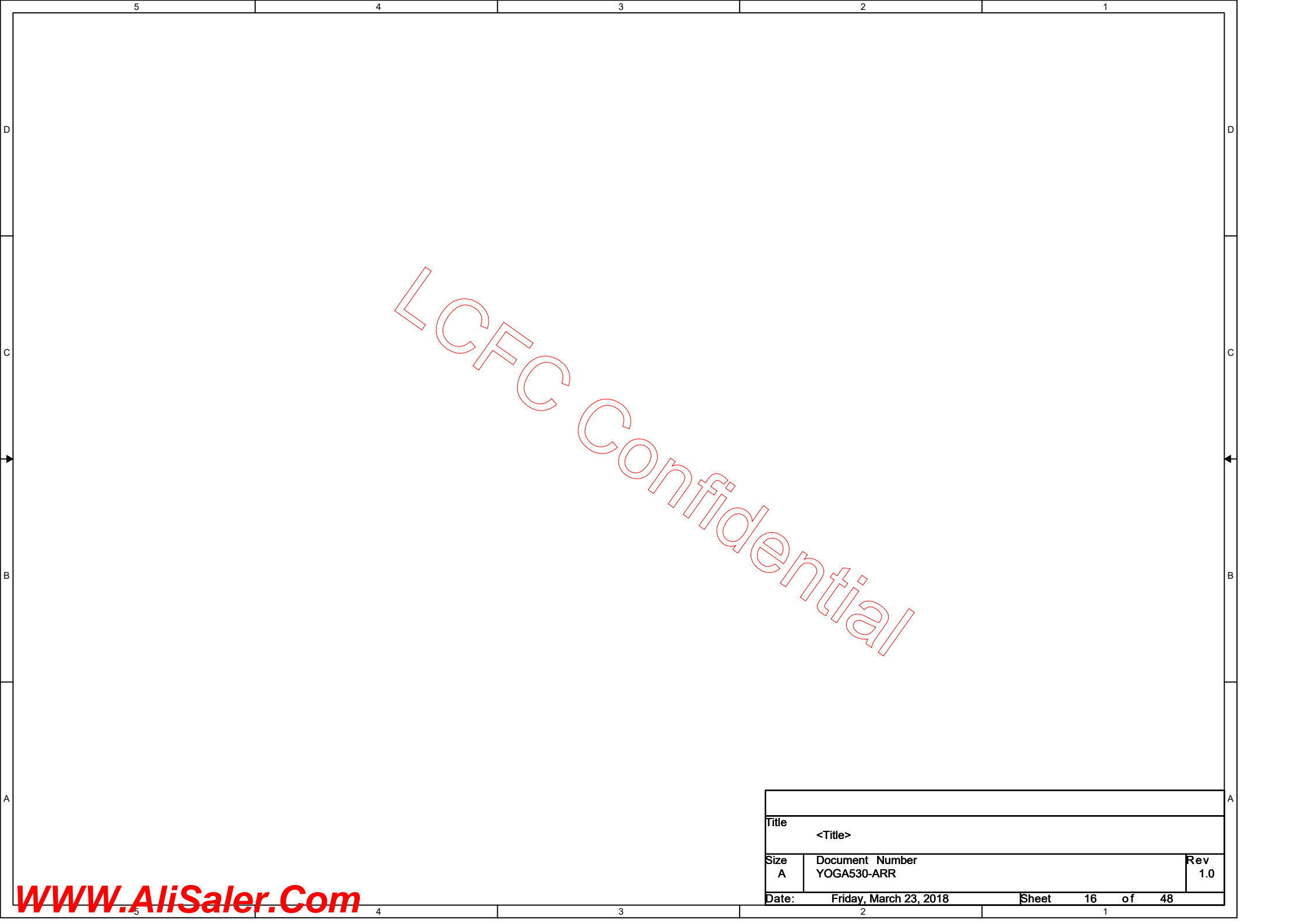
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D11	D11A D11B
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D59	D59A D59B
D60	D60A D60B
D61	D61A D61B
D62	D62A D62B
D63	D63A D63B
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D65	D65A D65B



Layout Note: Place near JDDR2



SPD Address = A4H



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Size	Document Number		Rev
A	YOGA530-ARR		1.0
Date:	Friday, March 23, 2018		Sheet 16 of 48

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Size A		Document Number YOGA530-ARR																				Rev 1.0		
Date:		Friday, March 23, 2018												Sheet		17		of		48				

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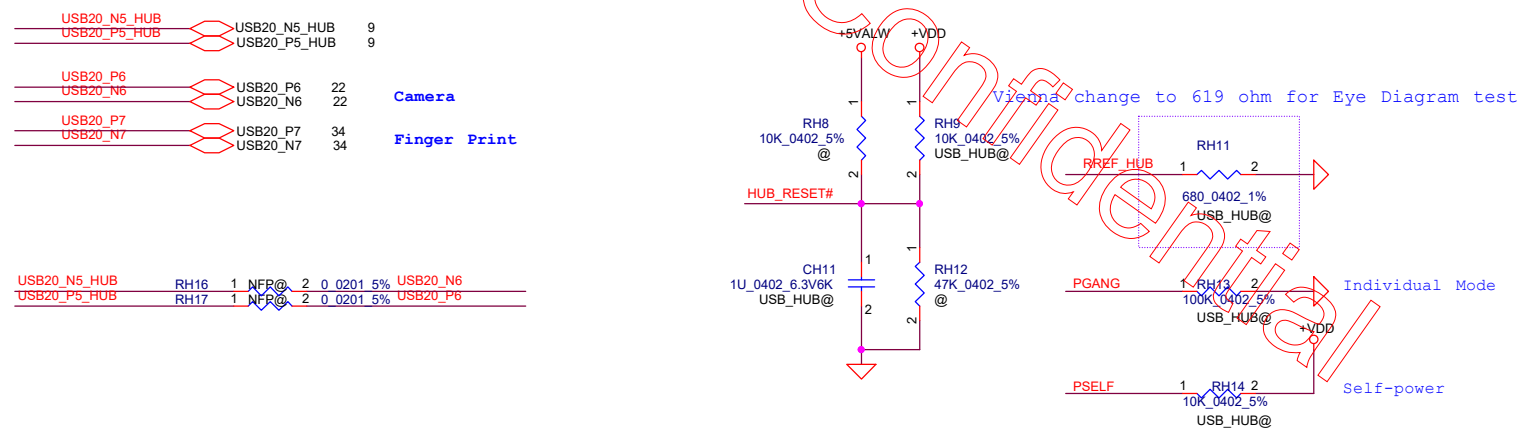
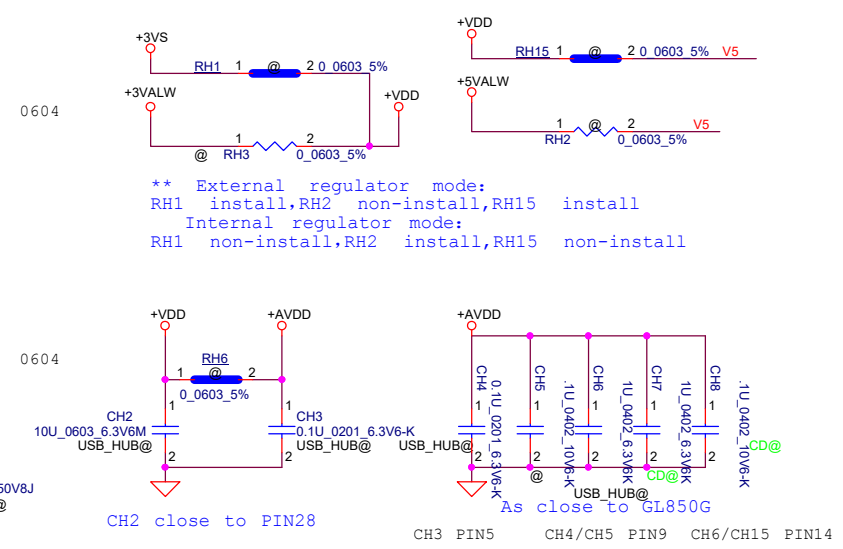
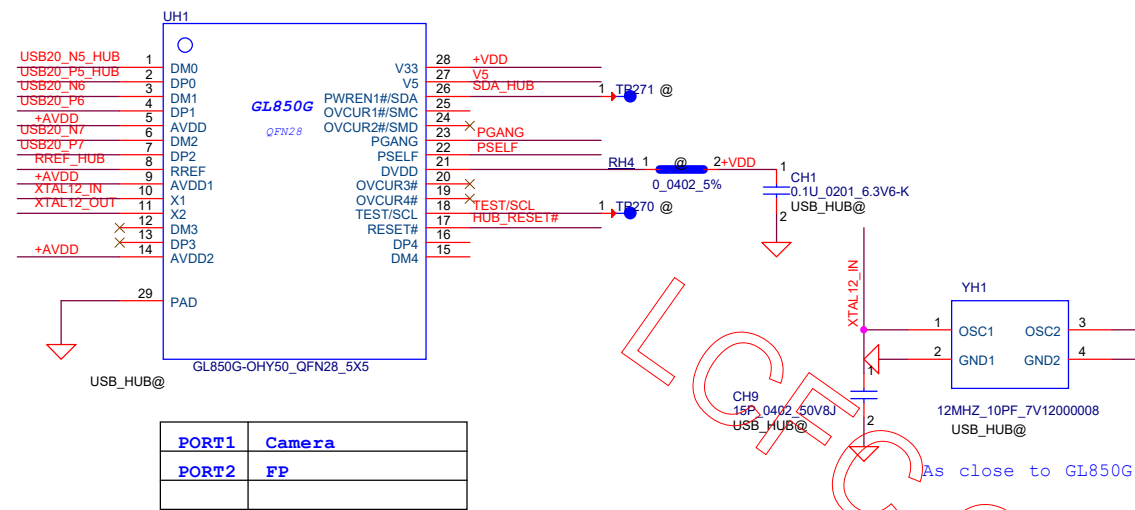
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Date:	Friday, March 23, 2018	Sheet 17 of 48	

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SizeA	Document NumberYOGA530-ARR		Rev1.0
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for USB HUB update to OHY50, manual modify PN to GL850G-OHY50

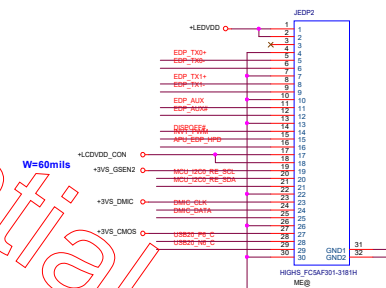
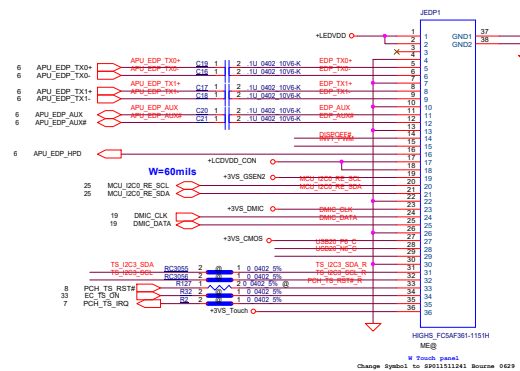
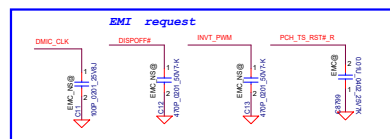
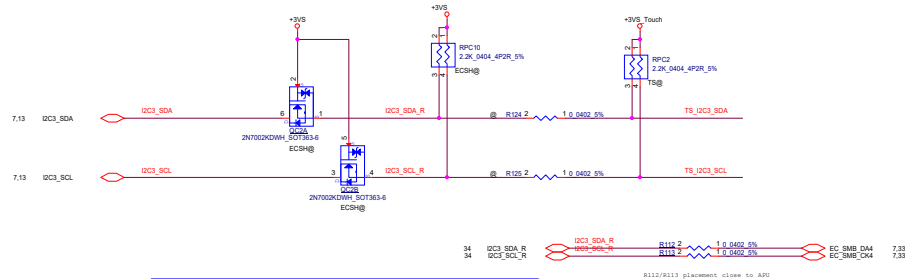
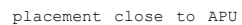
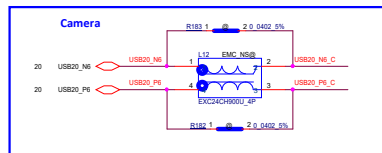
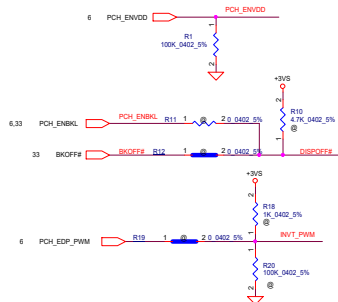
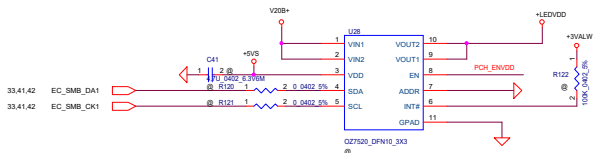
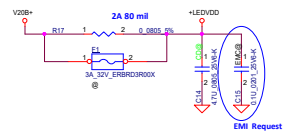


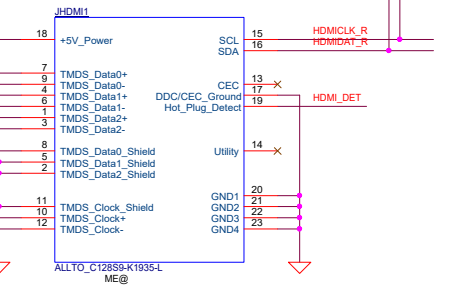
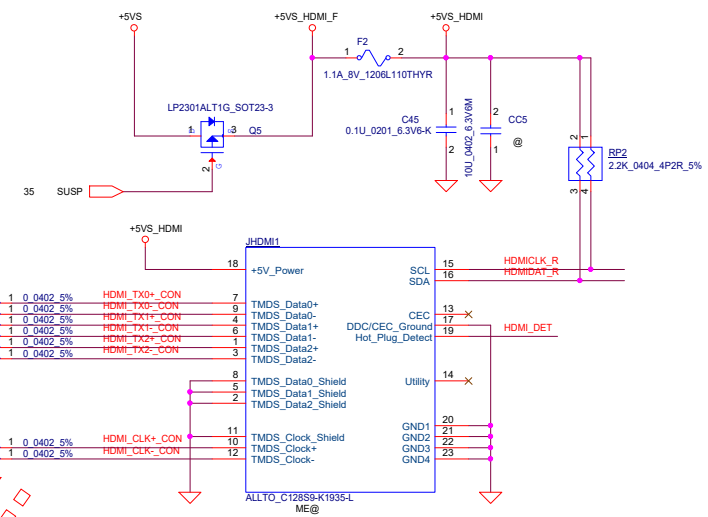
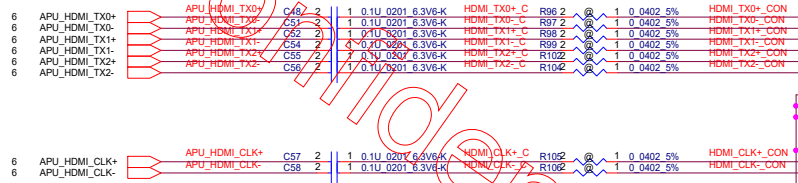
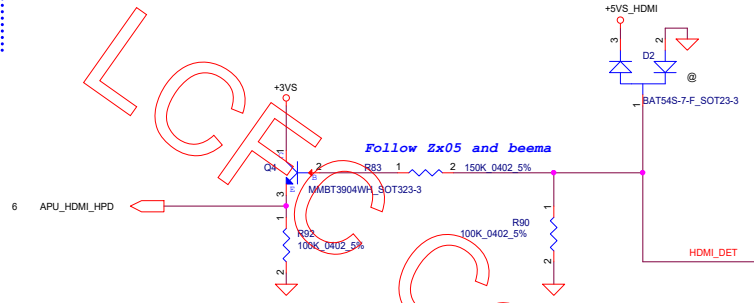
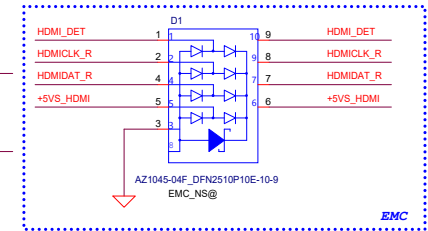
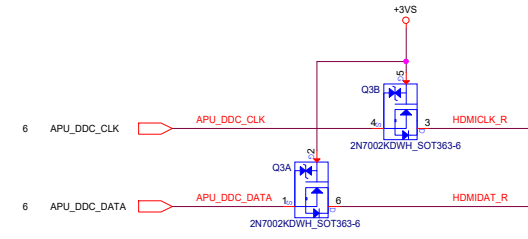
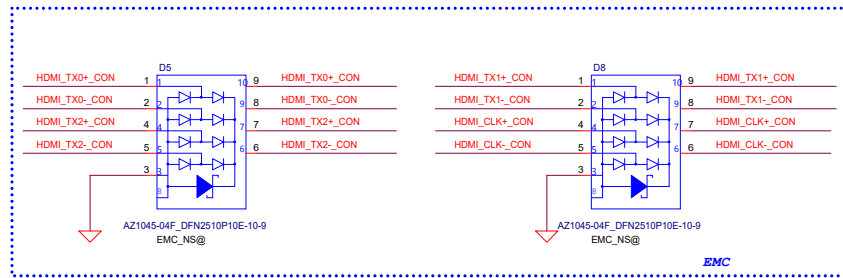
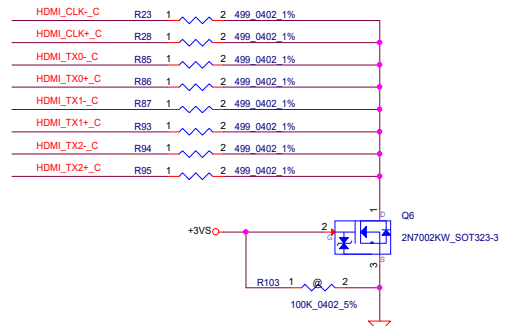
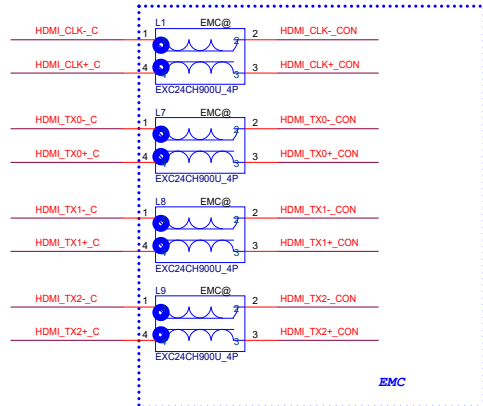
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THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.				Size B	Document Number
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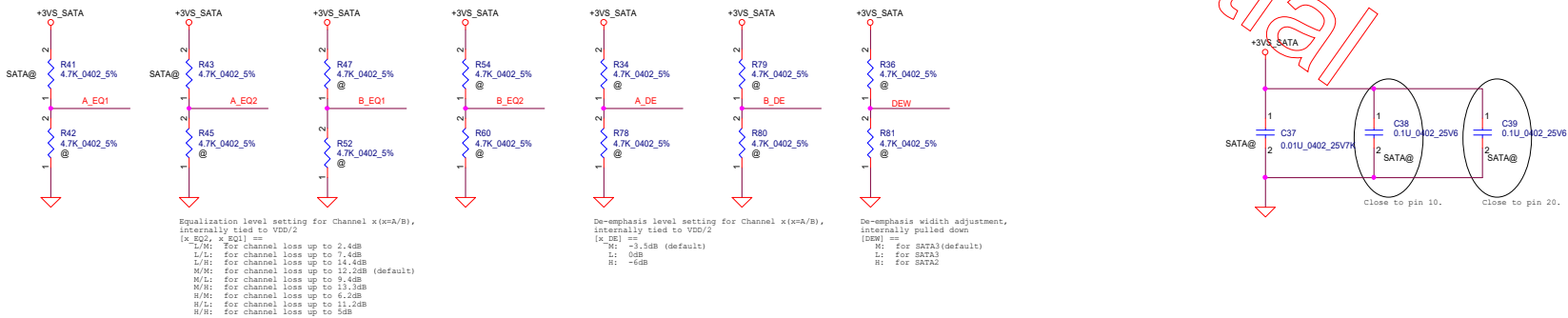
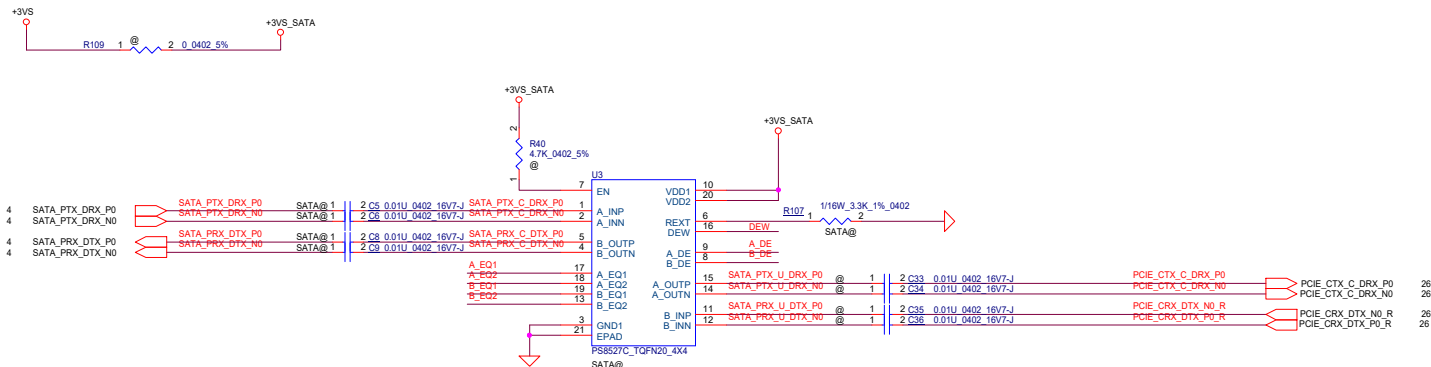
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Date:		Friday, March 23, 2018		Sheet	21 of 48	

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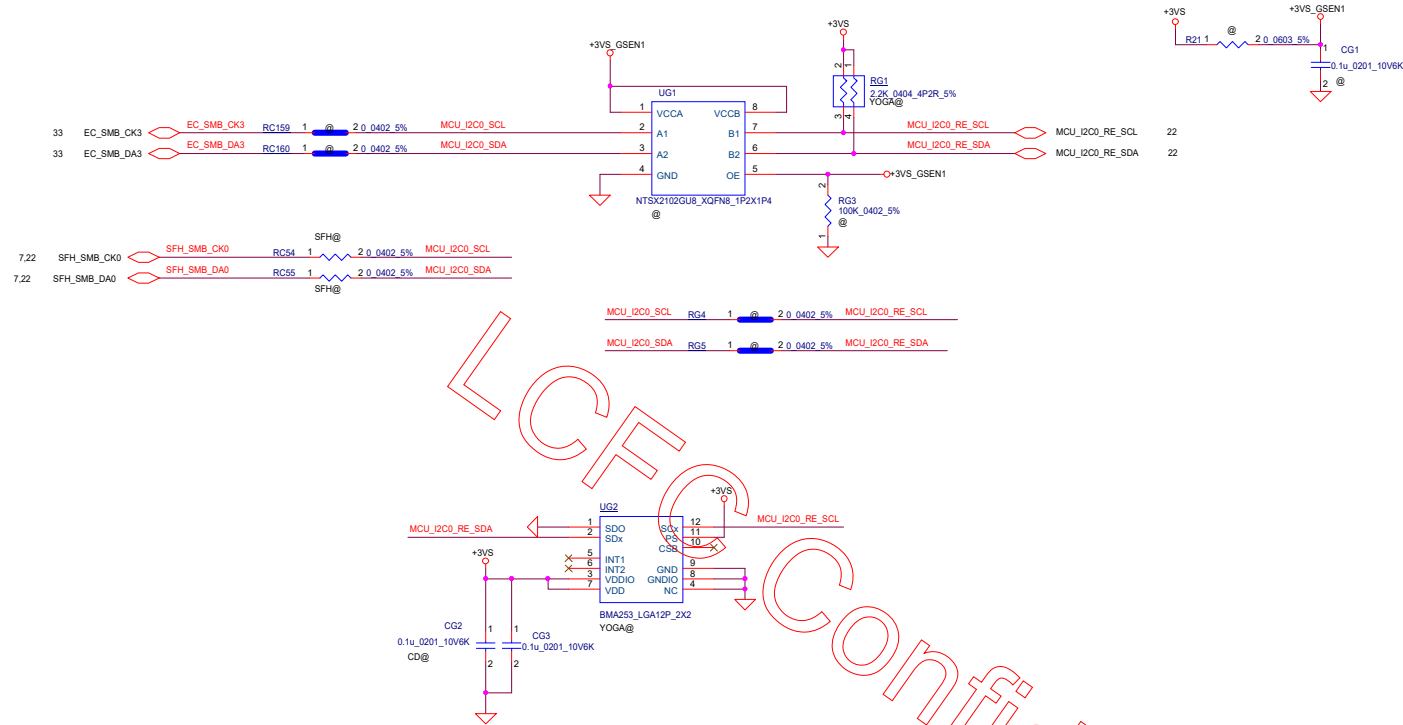
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SATA HDD Redriver

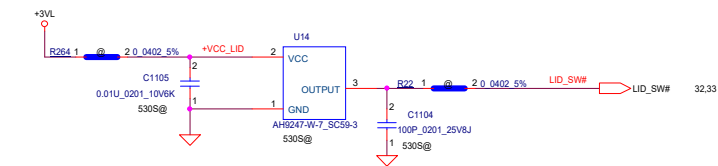


Follow Vendor suggest

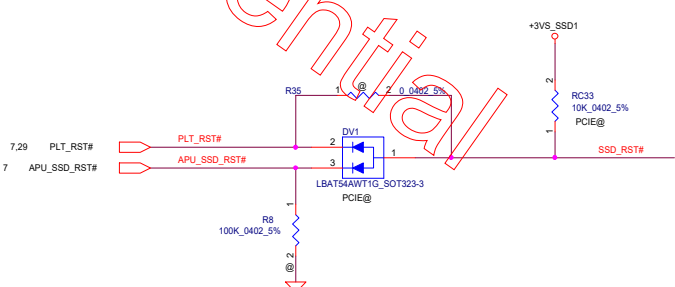
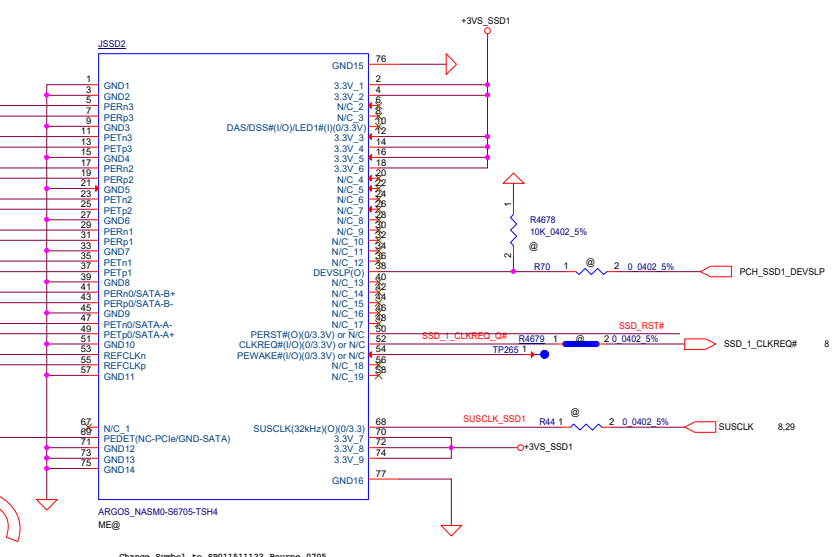
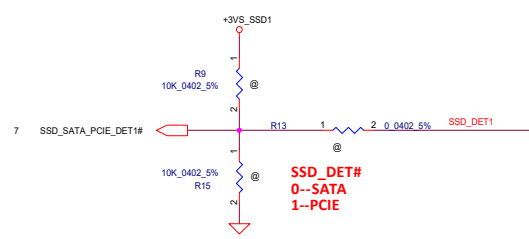
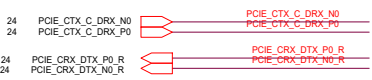
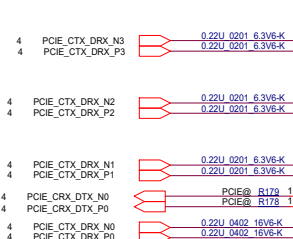
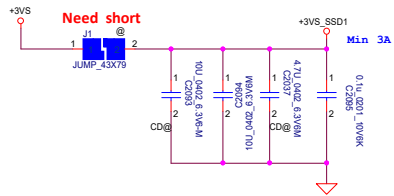
G-SENSOR



LID switch




Security Classification		LC Future Center Secret Data		Title	
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				Date:	Friday, March 28, 2016
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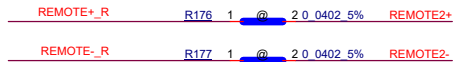


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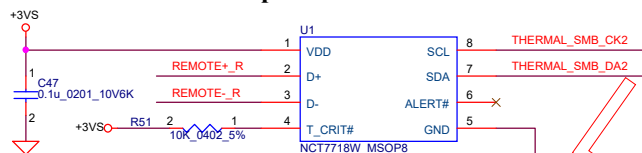
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Close to U1



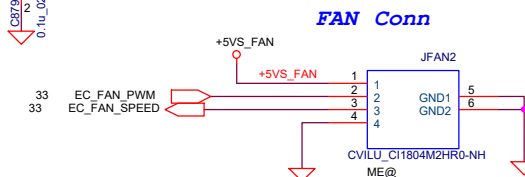
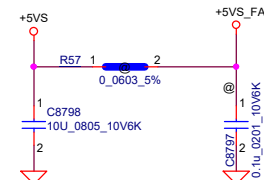
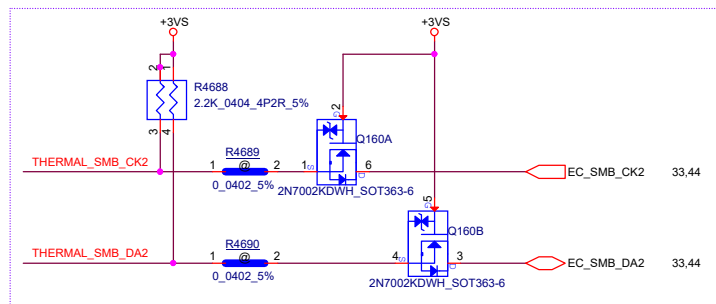
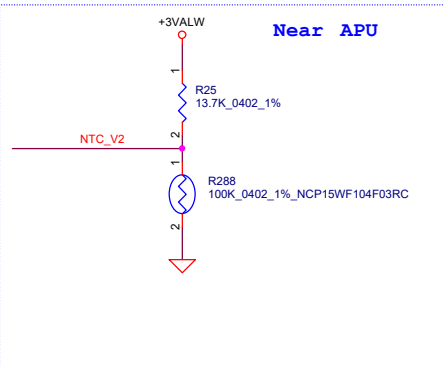
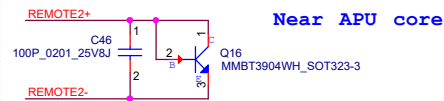
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Trace length:<8"

SMSC thermal sensor
placed near DIMM



Address 1001_101xb

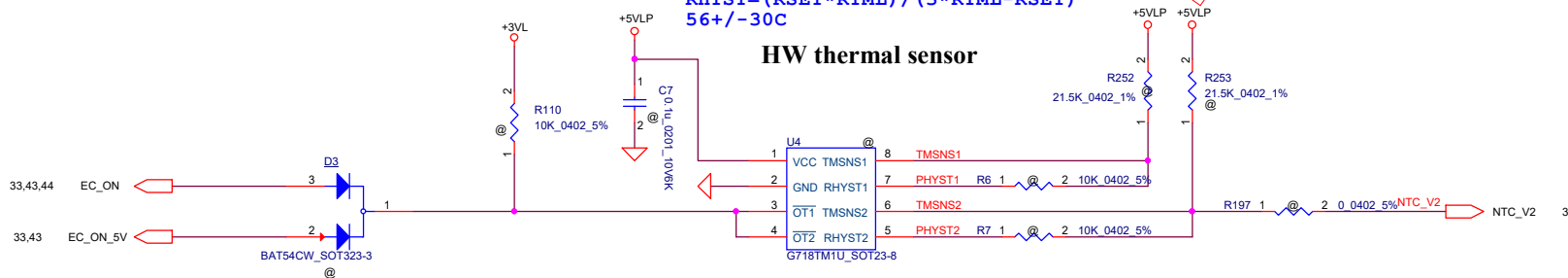
Near GPU&VRAM



Change Symbol to SP01001J000 Bourne 0629

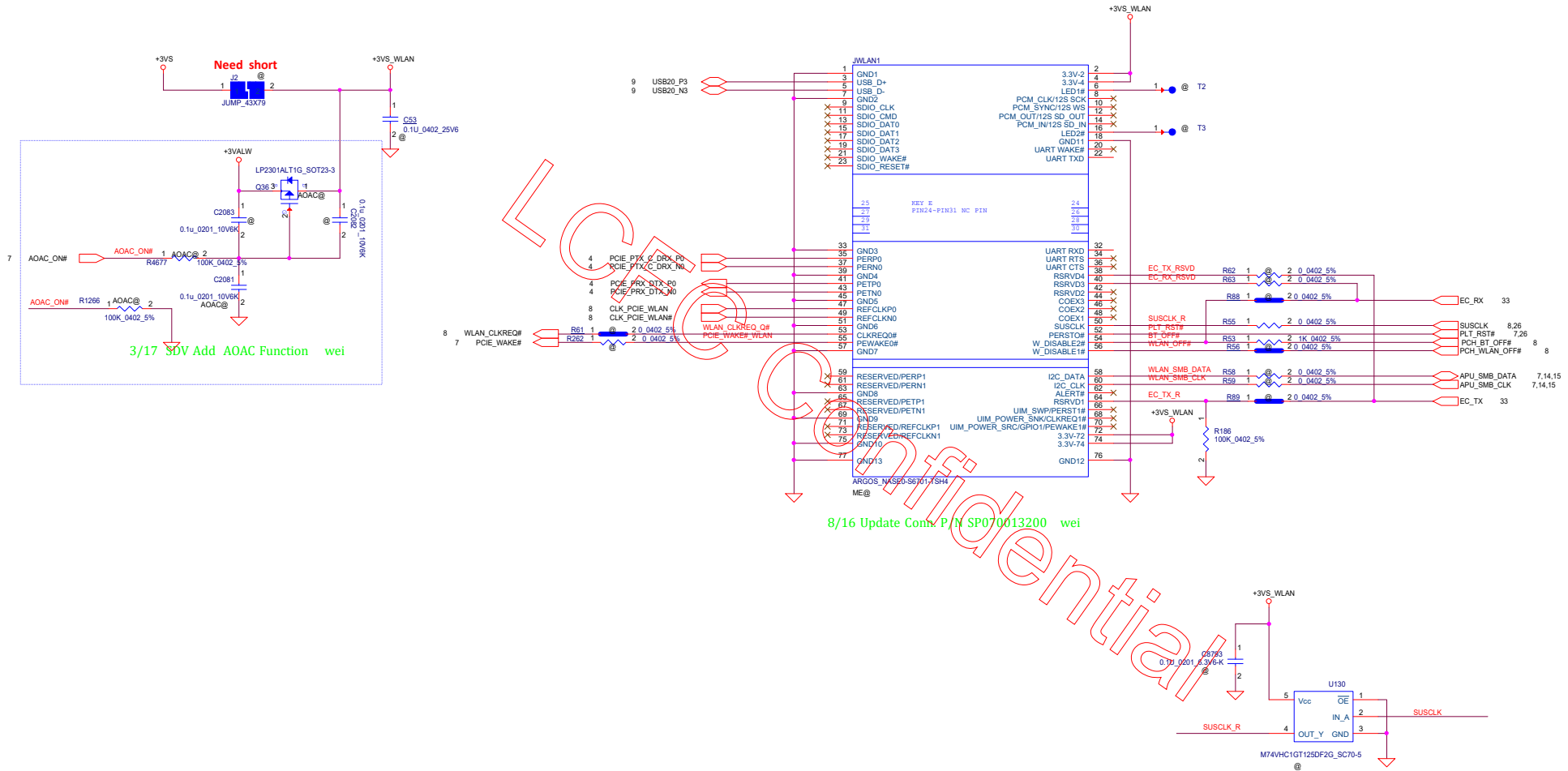
over temperature threshold:
RSET=3*RTMH
92+/-30C
Hysteresis temperature threshold.
RHYST= (RSET*RTML) / (3*RTML-RSET)
56+/-30C

HW thermal sensor



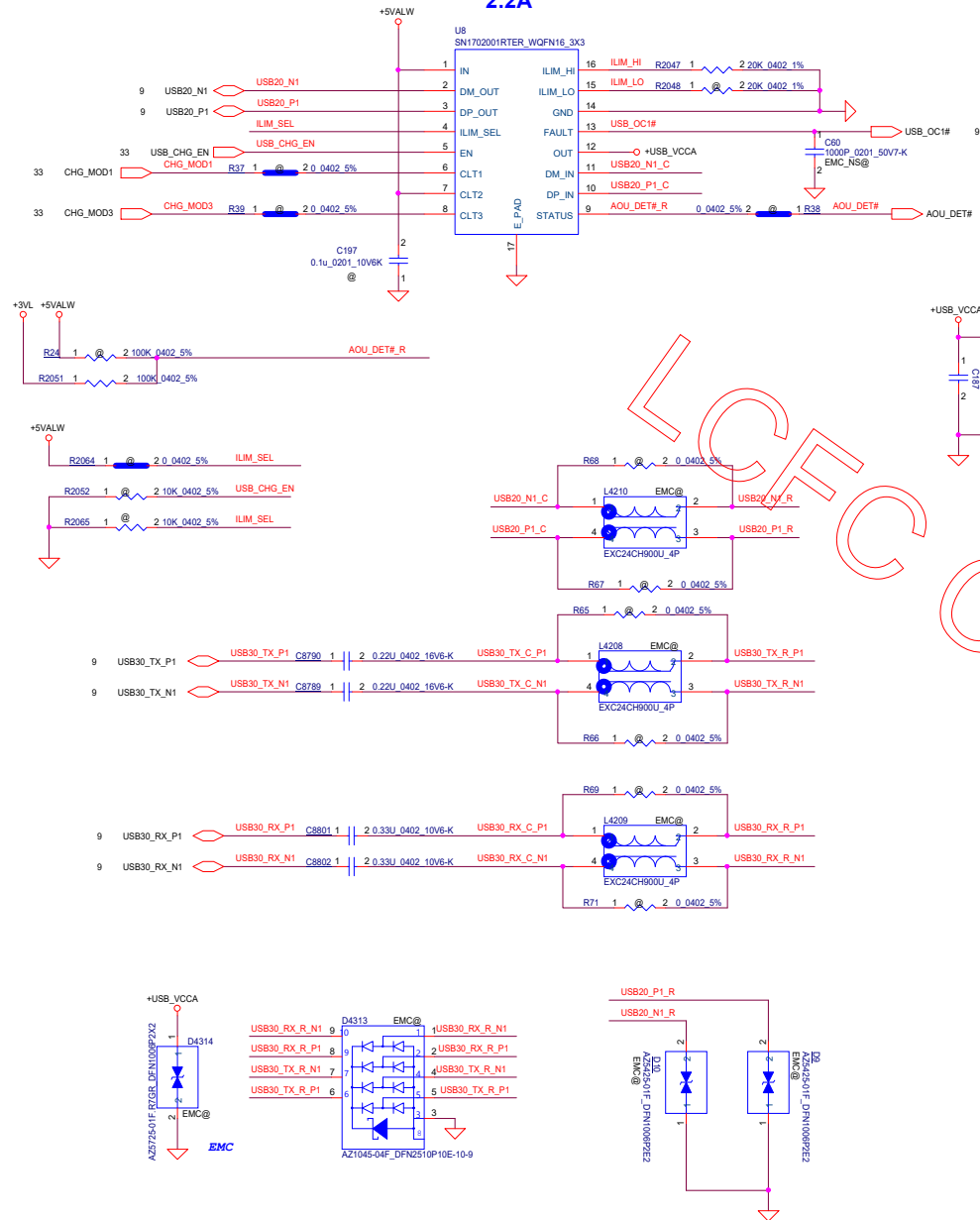
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Mini-Express Card(WLAN/WiMAX)

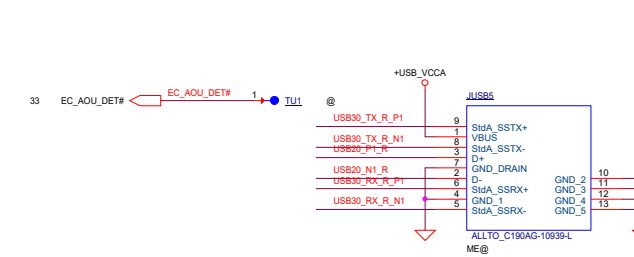


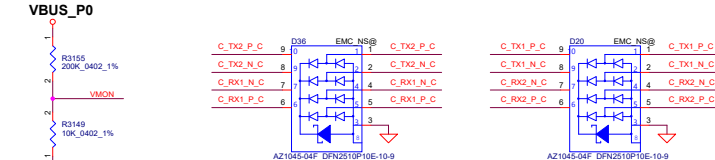
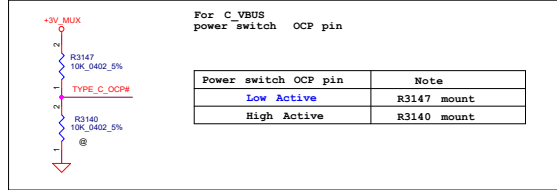
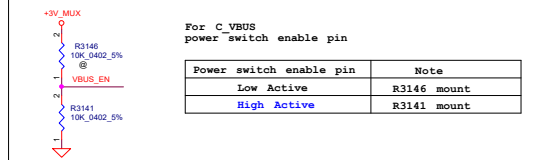
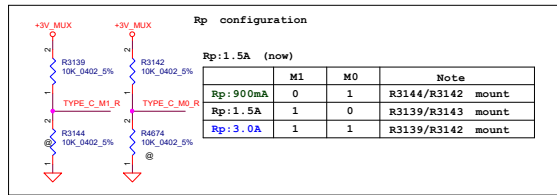
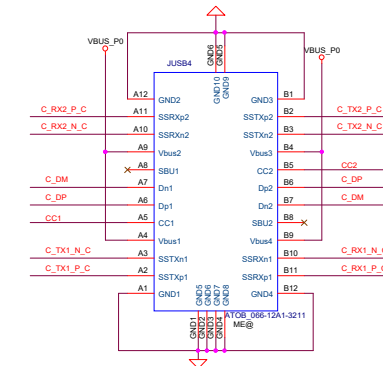
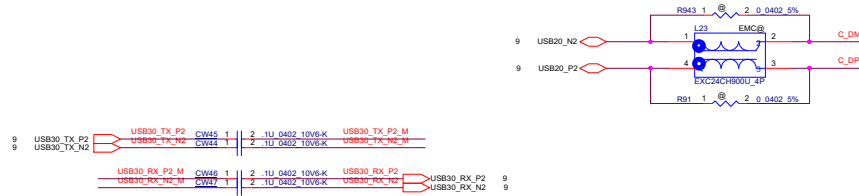
LEFT SIDE USB3.0 PORT x1

USB charger
2.2A

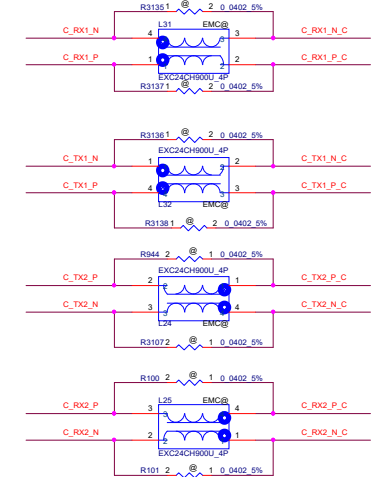
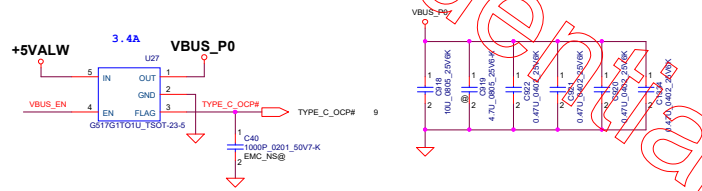
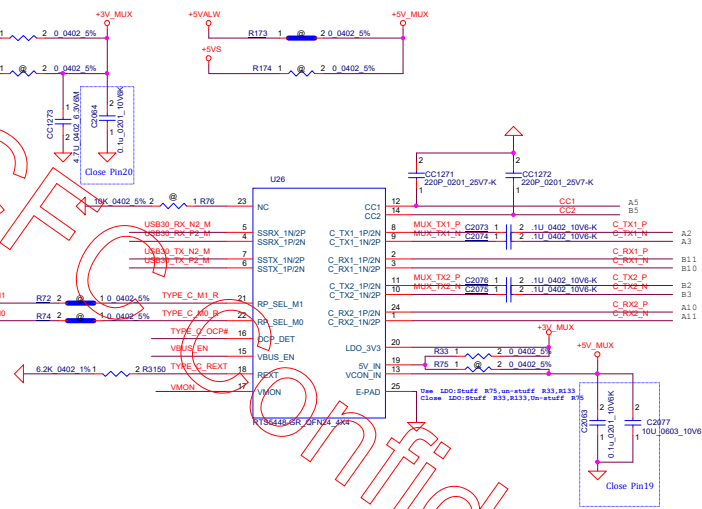


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1	1	1	1	CDP	Data Connected and Port Power Mgt. Function Active
1	1	1	0	SDP2	Data Connected
1	1	0	X	SDP1	Data Connected
0	1	0	X	SDP1	Data Connected
1	0	0	X	DCP_Short	Device Forced to stay in DCP BC 1.2 charging mode
1	0	1	X	DCP_Divider	Device Forced to stay in DCP Divider 1 Charging Mode
0	1	1	X	DCP_Auto	Data Disconnected and Port Power Mgt. Function Active
0	0	1	X	DCP_Auto	Data Disconnected and Power Wake Function Active



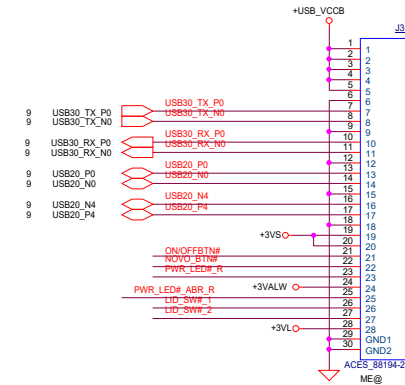
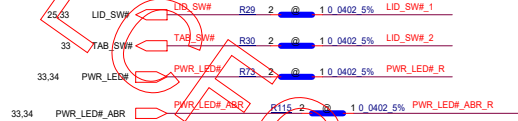
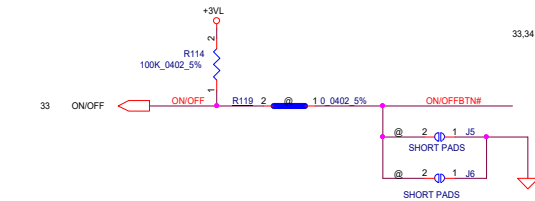
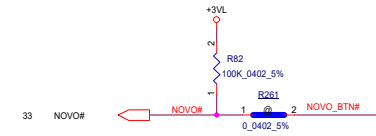
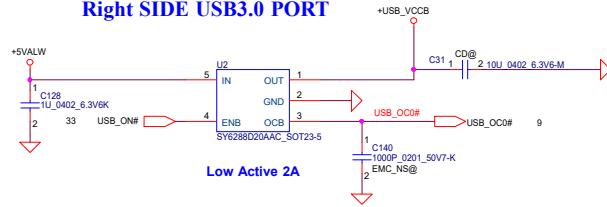


For ESD



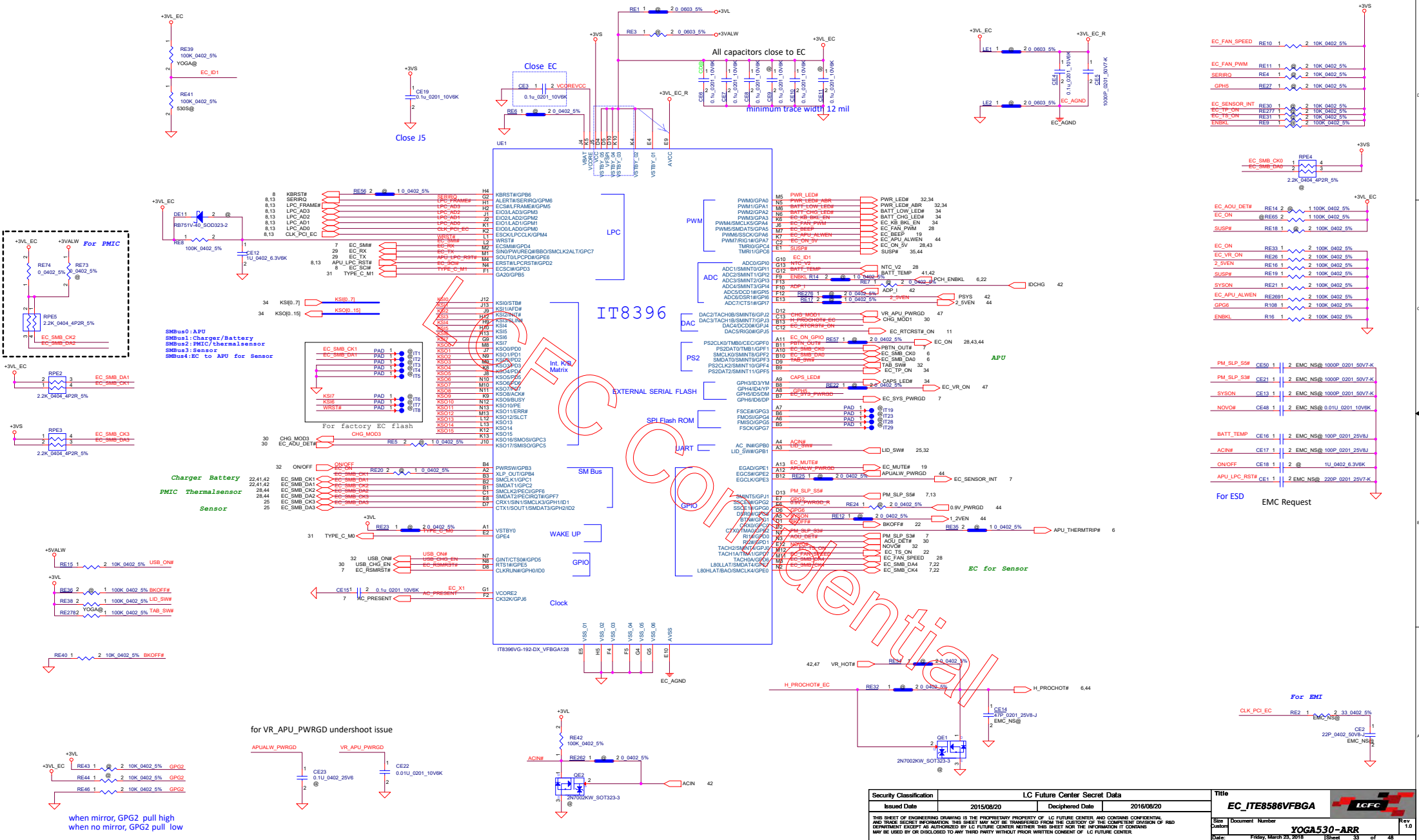
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31		31		48	

Right SIDE USB3.0 PORT



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when mirror, GPG2 pull high
when no mirror, GPG2 pull low

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ZZZ4

AMD Ryzen 7 2700U 2.2G/4C/6M/FP5
RT@
SA00008QB10

ZZZ2

AMD Ryzen 5 2500U 2.0G/4C/6M/FP5
RC@
SA00008QA10

ZZZ3

RAVEN RIDGE YM2500C4T4MFBA
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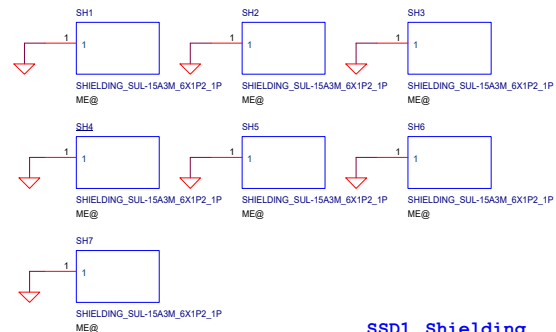
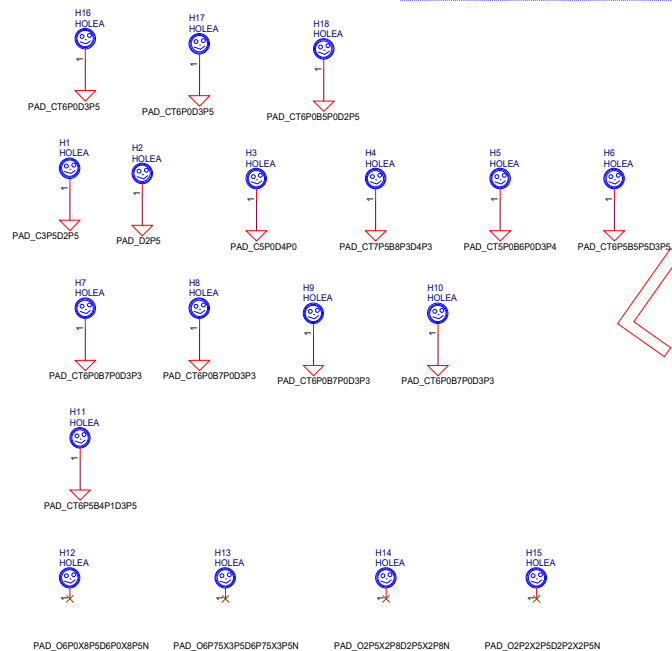
APU type

ZZZ1

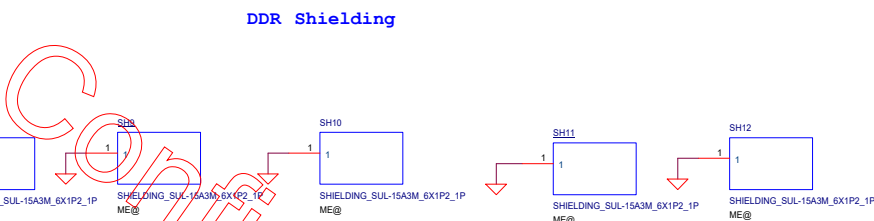
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DA800011R00
DA8@

PCB_MB

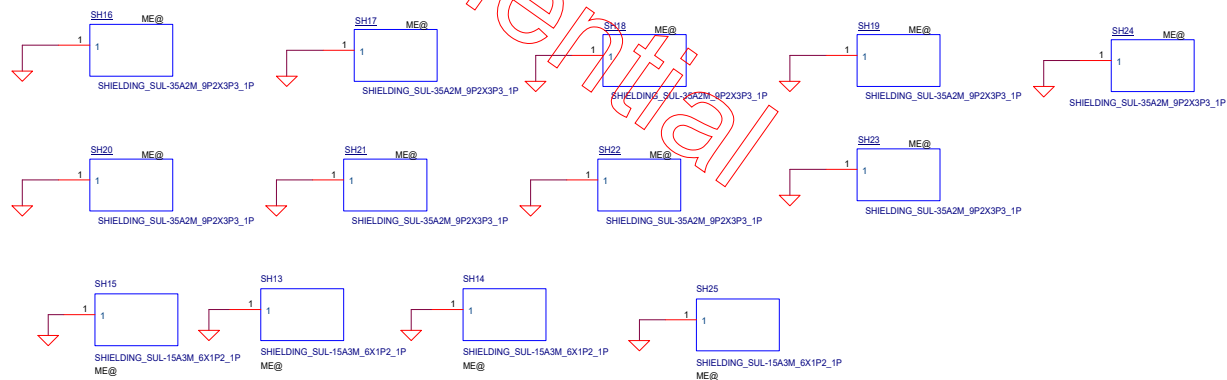
PCB Fedical Mark PAD




SSD1 Shielding




DDR Shielding

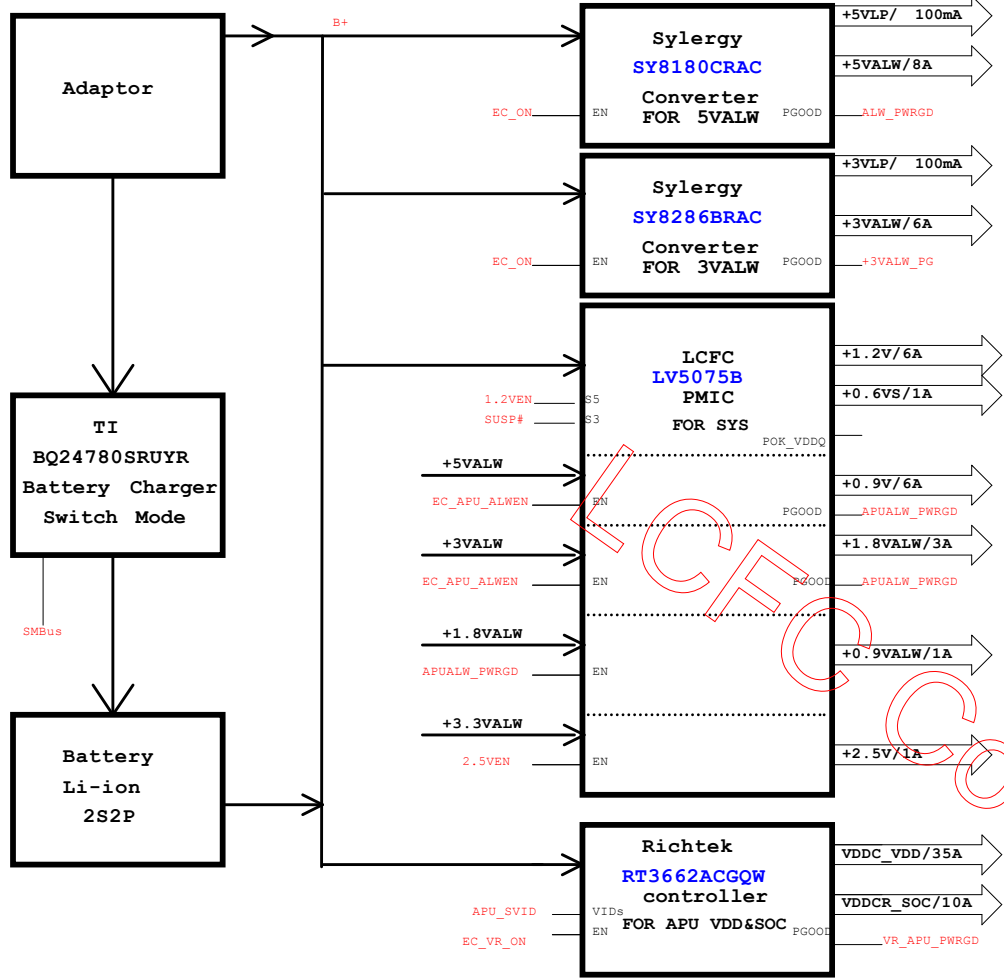


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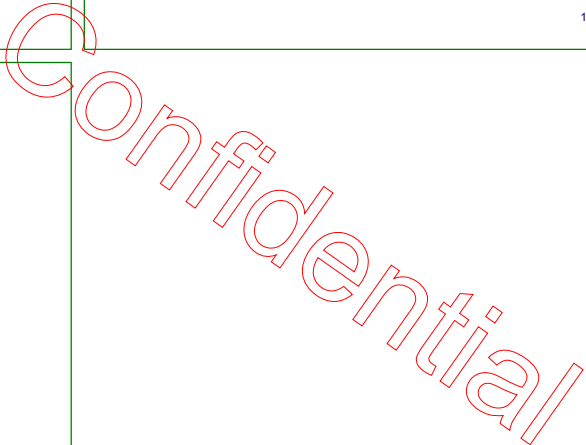
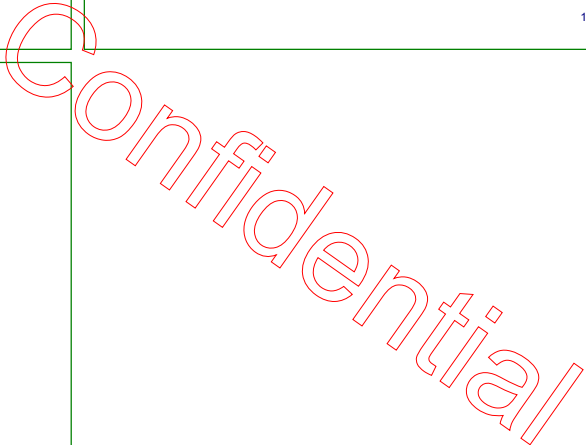
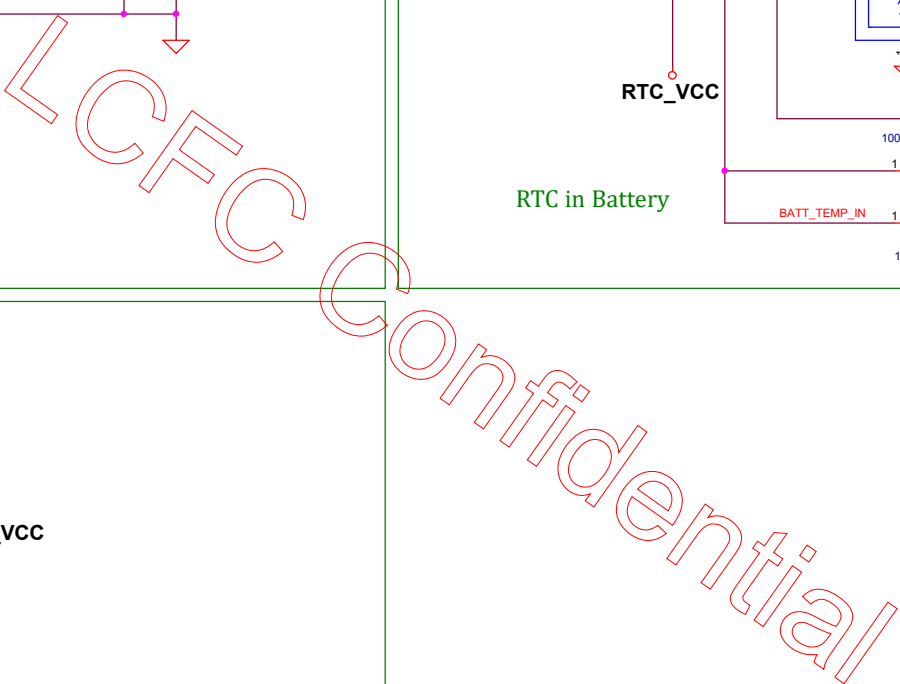
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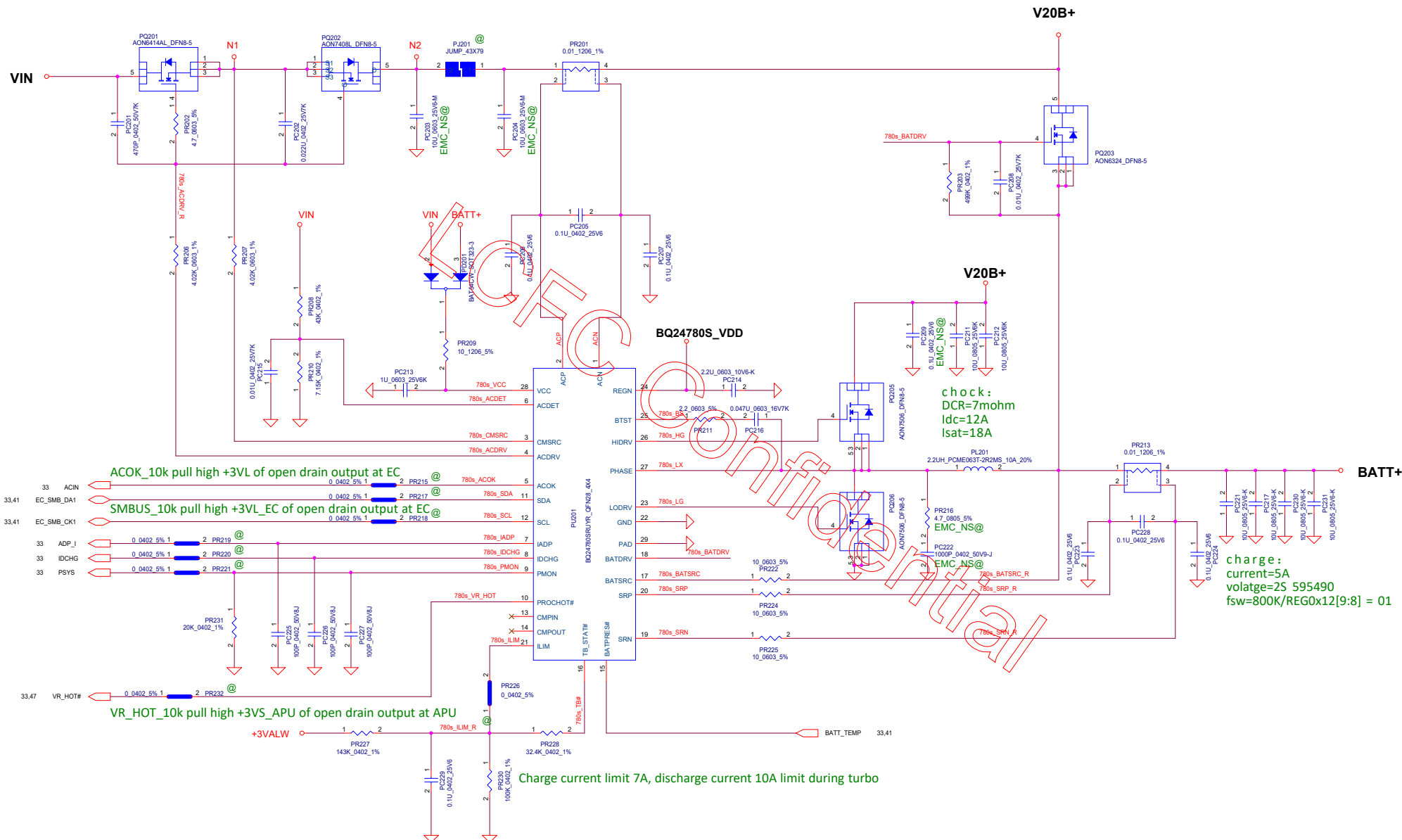


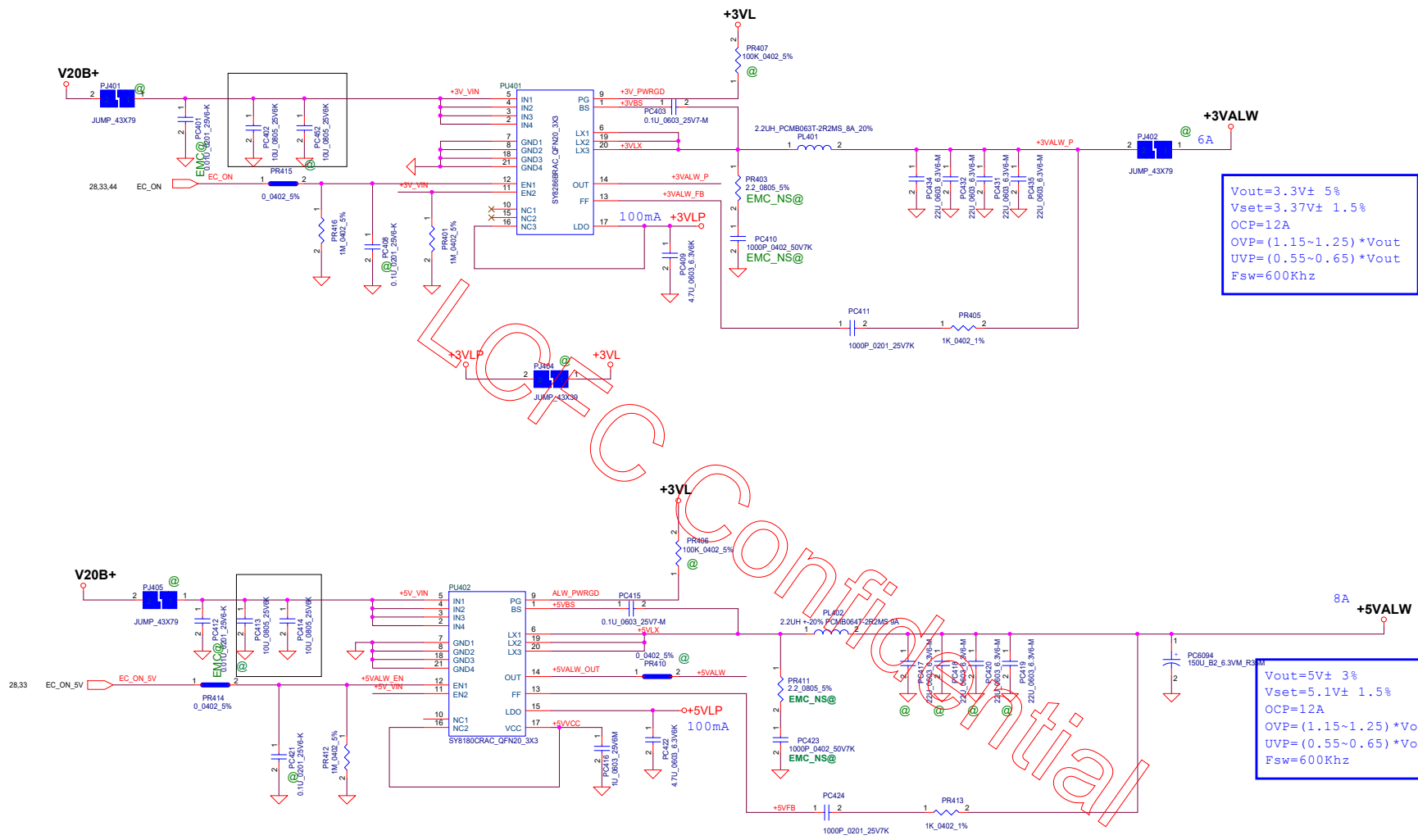
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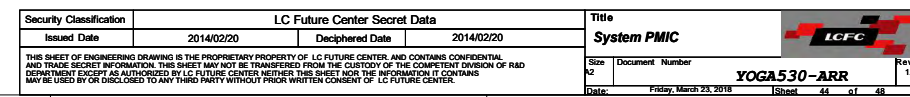









$V_{out}=3.3V \pm 5\%$
 $V_{set}=3.37V \pm 1.5\%$
 $OCP=12A$
 $OVP=(1.15 \sim 1.25) * V_{out}$
 $UVP=(0.55 \sim 0.65) * V_{out}$
 $F_{sw}=600Khz$

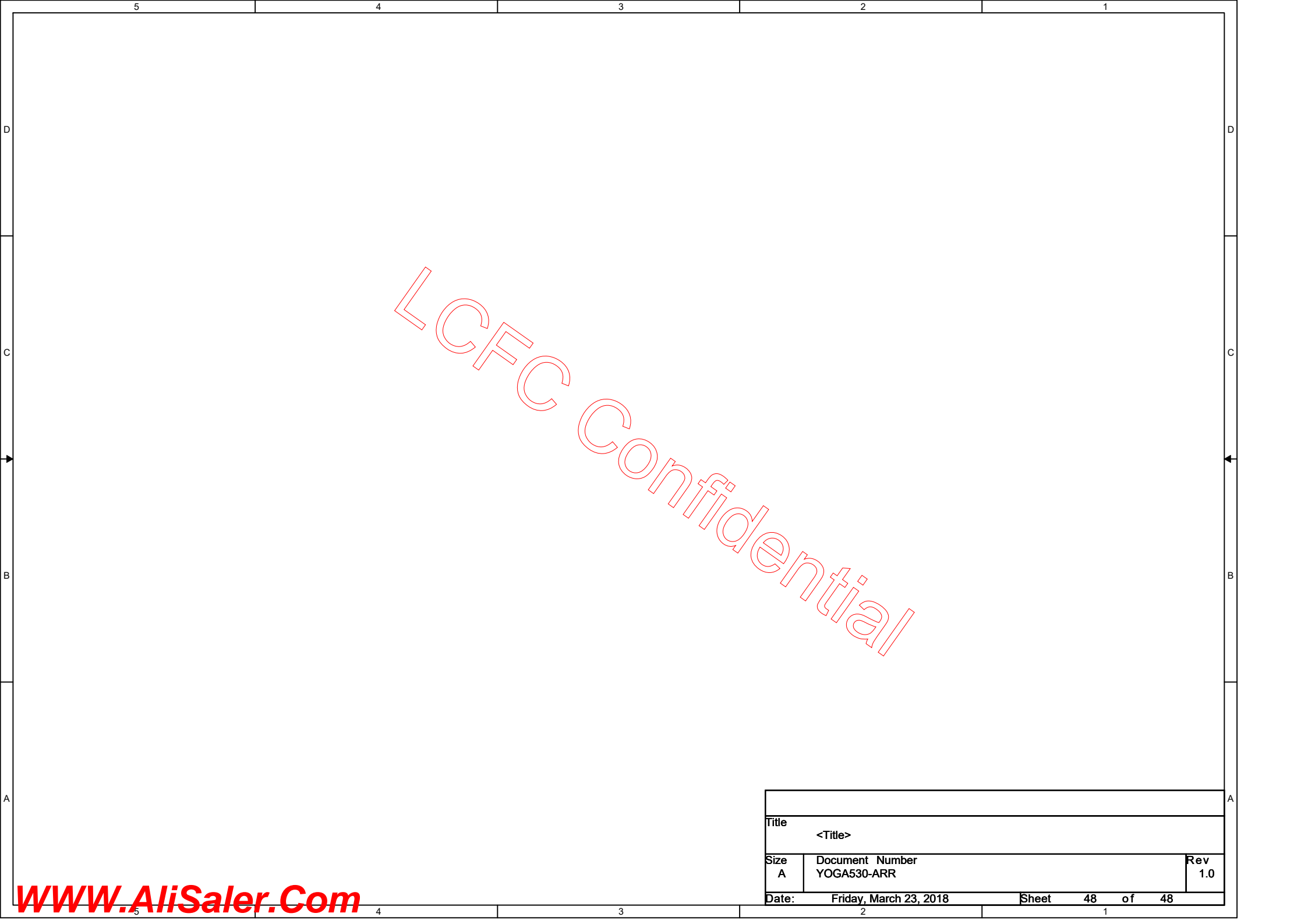
$V_{out}=5V \pm 3\%$
 $V_{set}=5.1V \pm 1.5\%$
 $OCP=12A$
 $OVP=(1.15 \sim 1.25) * V_{out}$
 $UVP=(0.55 \sim 0.65) * V_{out}$
 $F_{sw}=600Khz$



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